FIG. 1

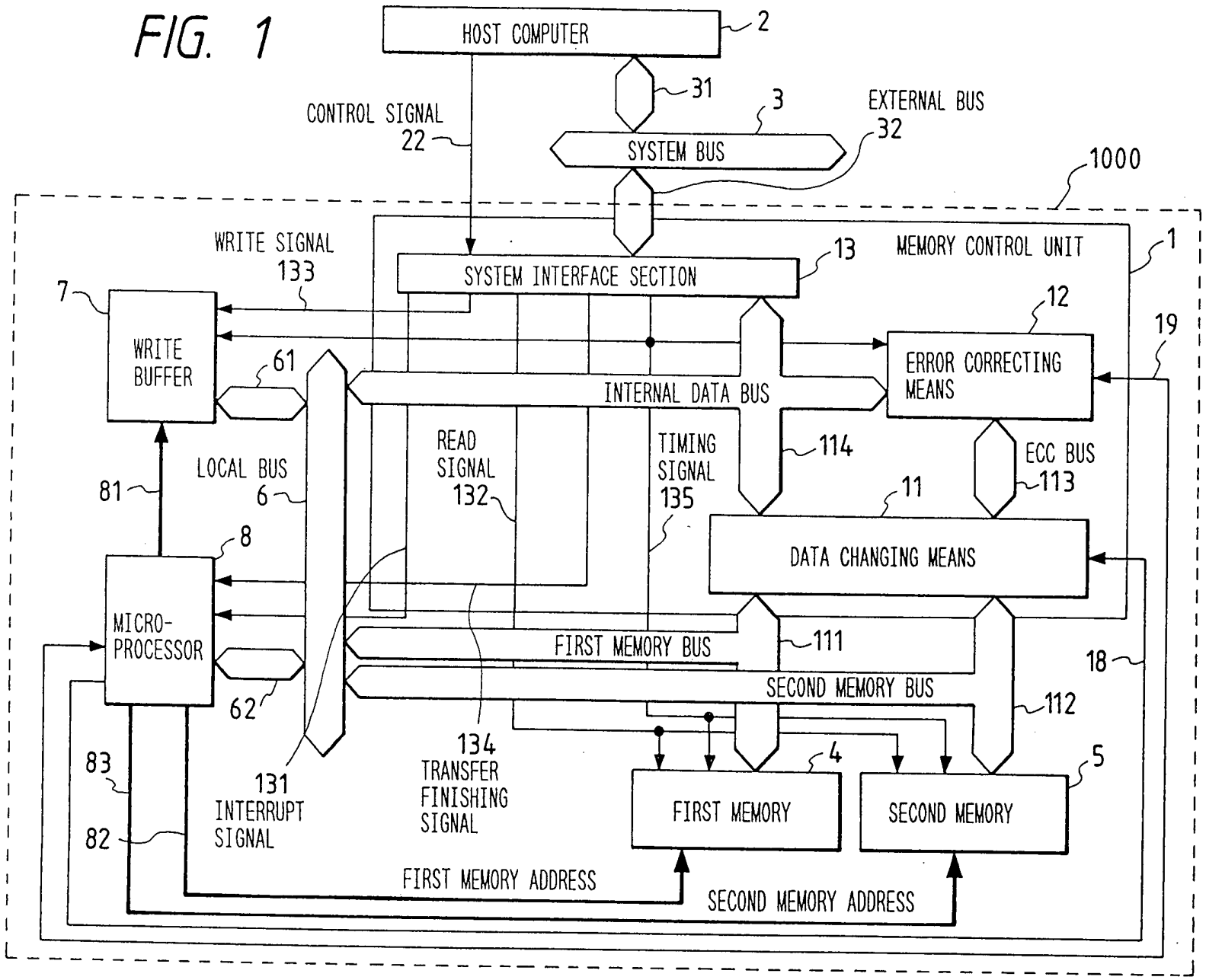
HOST COMPUTER
2
31
3
EXTERNAL BUS
32
CONTROL SIGNAL
22
SYSTEM BUS
1000
WRITE SIGNAL
133
SYSTEM INTERFACE SECTION
13
MEMORY CONTROL UNIT
1
7
WRITE BUFFER
61
12
ERROR CORRECTING MEANS
19
INTERNAL DATA BUS
READ SIGNAL
132
TIMING SIGNAL
135
114
ECC BUS
113
LOCAL BUS
6
81
11
DATA CHANGING MEANS
8
MICRO-PROCESSOR
FIRST MEMORY BUS
111
18
SECOND MEMORY BUS
112
62
83
131
INTERRUPT SIGNAL
134
TRANSFER FINISHING SIGNAL
4
5
FIRST MEMORY
SECOND MEMORY
82
FIRST MEMORY ADDRESS
SECOND MEMORY ADDRESS

FIG. 2

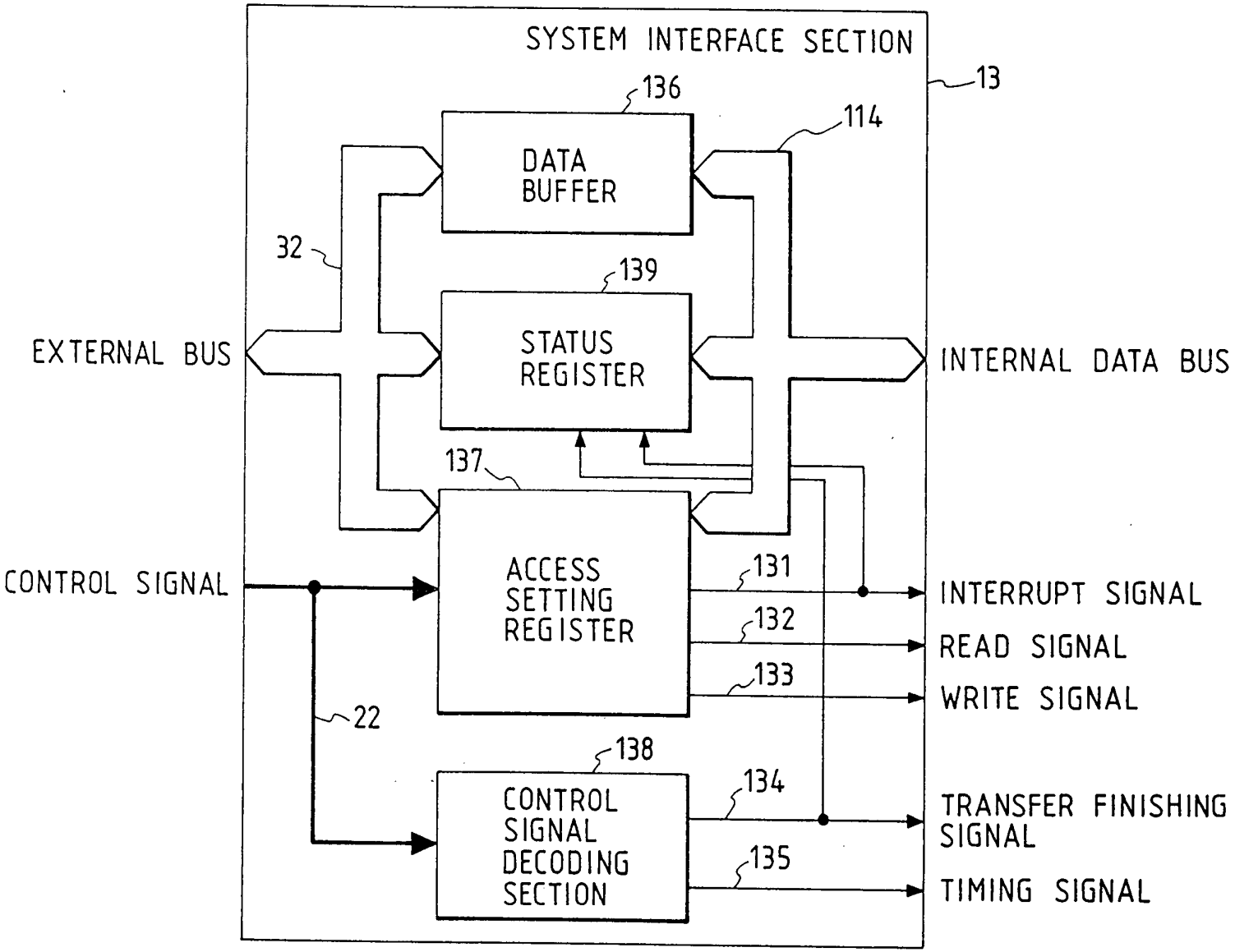
SYSTEM INTERFACE SECTION
13
136
DATA BUFFER
114
32
139
STATUS REGISTER
EXTERNAL BUS
INTERNAL DATA BUS
137
ACCESS SETTING REGISTER
CONTROL SIGNAL
131
INTERRUPT SIGNAL
132
READ SIGNAL
133
WRITE SIGNAL
22
138
CONTROL SIGNAL DECODING SECTION
134
TRANSFER FINISHING SIGNAL
135
TIMING SIGNAL

FIG. 3

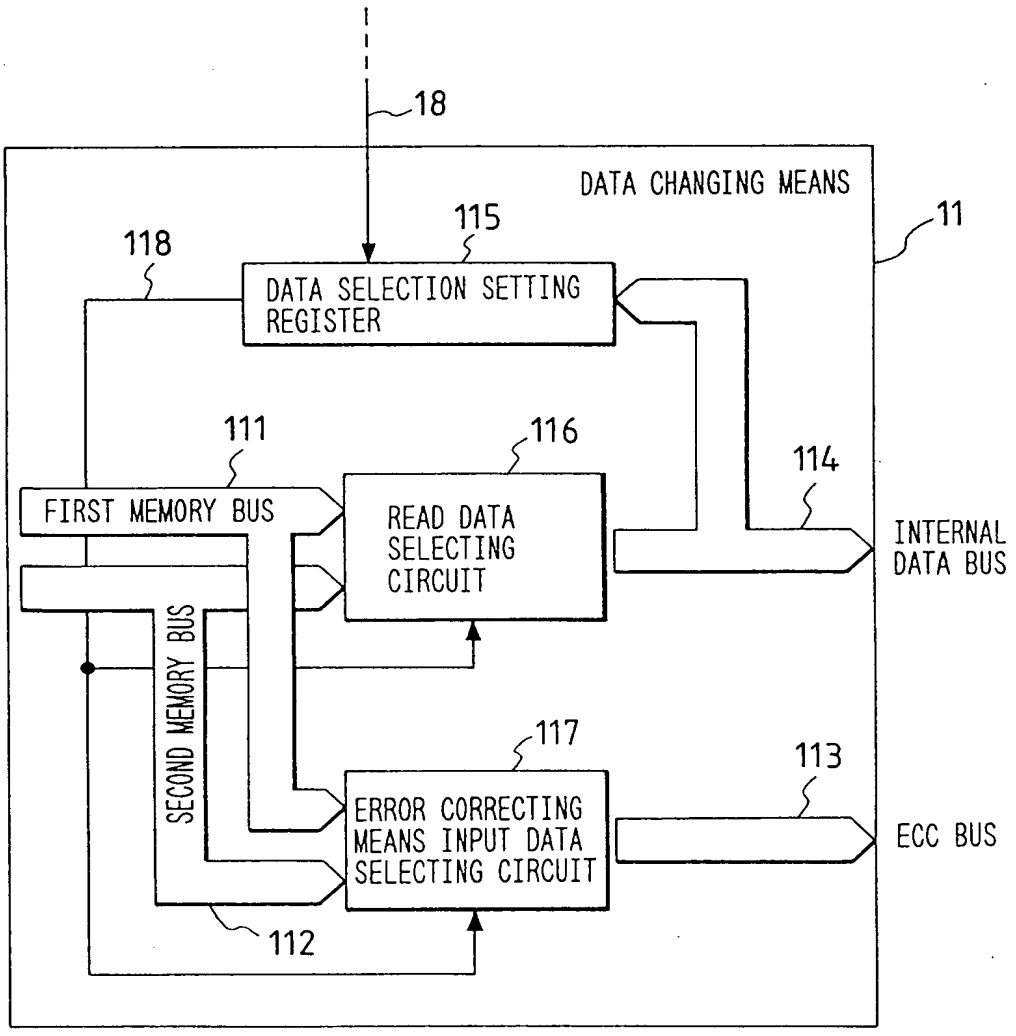
18
DATA CHANGING MEANS
11
115
118
DATA SELECTION SETTING REGISTER
111
116
114
FIRST MEMORY BUS
READ DATA SELECTING CIRCUIT
INTERNAL DATA BUS
SECOND MEMORY BUS
117
113
ERROR CORRECTING MEANS INPUT DATA SELECTING CIRCUIT
ECC BUS
112

FIG. 4

(SELECTING CIRCUIT (116))

DATA SELECTION SETTING REGISTER 115	INTERNAL DATA BUS 114
0	FIRST MEMORY BUS 111
1	SECOND MEMORY BUS 112

FIG. 5

(SELECTING CIRCUIT (117))

DATA SELECTION SETTING REGISTER 115	EEC BUS 113
0	FIRST MEMORY BUS 112
1	SECOND MEMORY BUS 111

FIG. 6

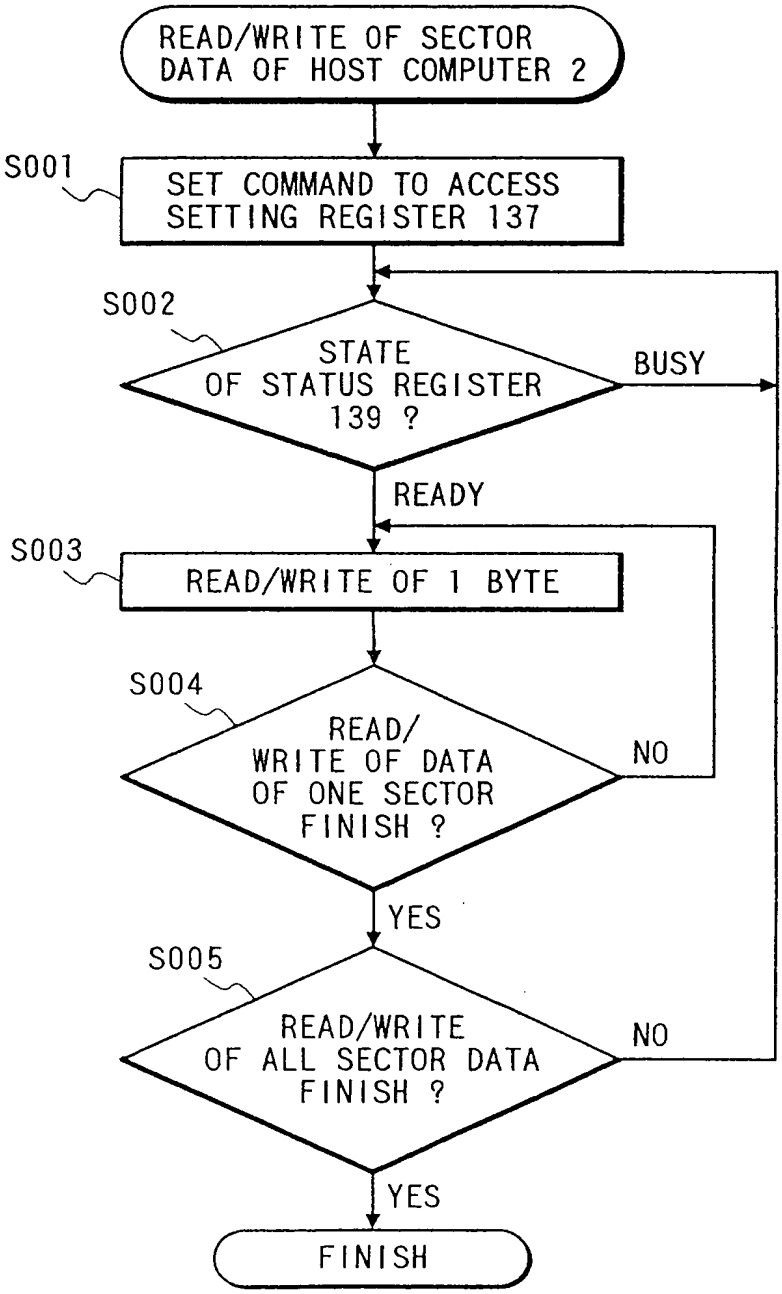
READ/WRITE OF SECTOR DATA OF HOST COMPUTER 2
S001
SET COMMAND TO ACCESS SETTING REGISTER 137
S002
STATE OF STATUS REGISTER 139 ?
BUSY
READY
S003
READ/WRITE OF 1 BYTE
S004
READ/ WRITE OF DATA OF ONE SECTOR FINISH ?
NO
YES
S005
READ/WRITE OF ALL SECTOR DATA FINISH ?
NO
YES
FINISH

FIG. 7

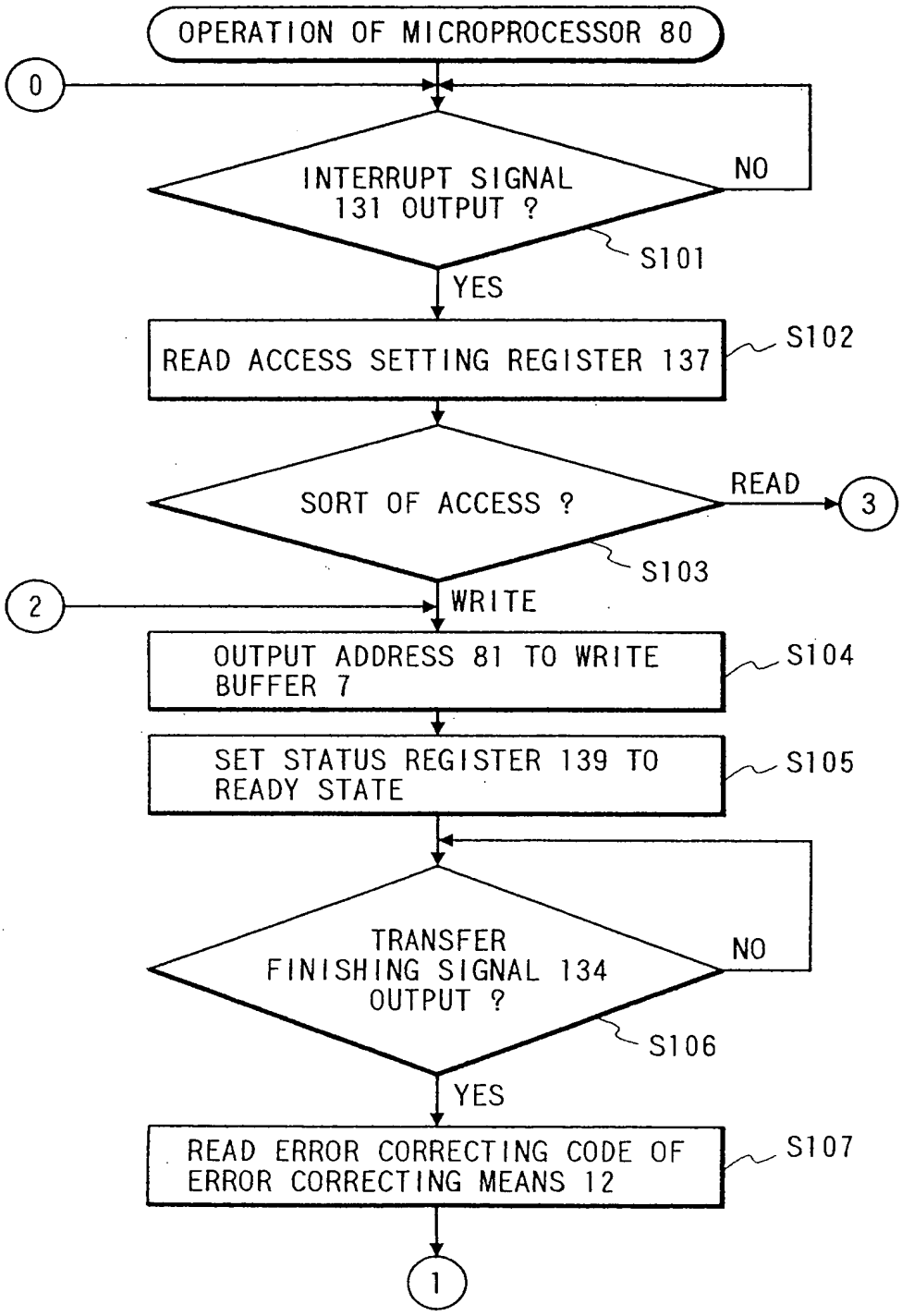
OPERATION OF MICROPROCESSOR 80
0
INTERRUPT SIGNAL 131 OUTPUT ?
NO
S101
YES
READ ACCESS SETTING REGISTER 137
S102
SORT OF ACCESS ?
READ
3
S103
2
WRITE
OUTPUT ADDRESS 81 TO WRITE BUFFER 7
S104
SET STATUS REGISTER 139 TO READY STATE
S105
TRANSFER FINISHING SIGNAL 134 OUTPUT ?
NO
S106
YES
READ ERROR CORRECTING CODE OF ERROR CORRECTING MEANS 12
S107
1

FIG. 8

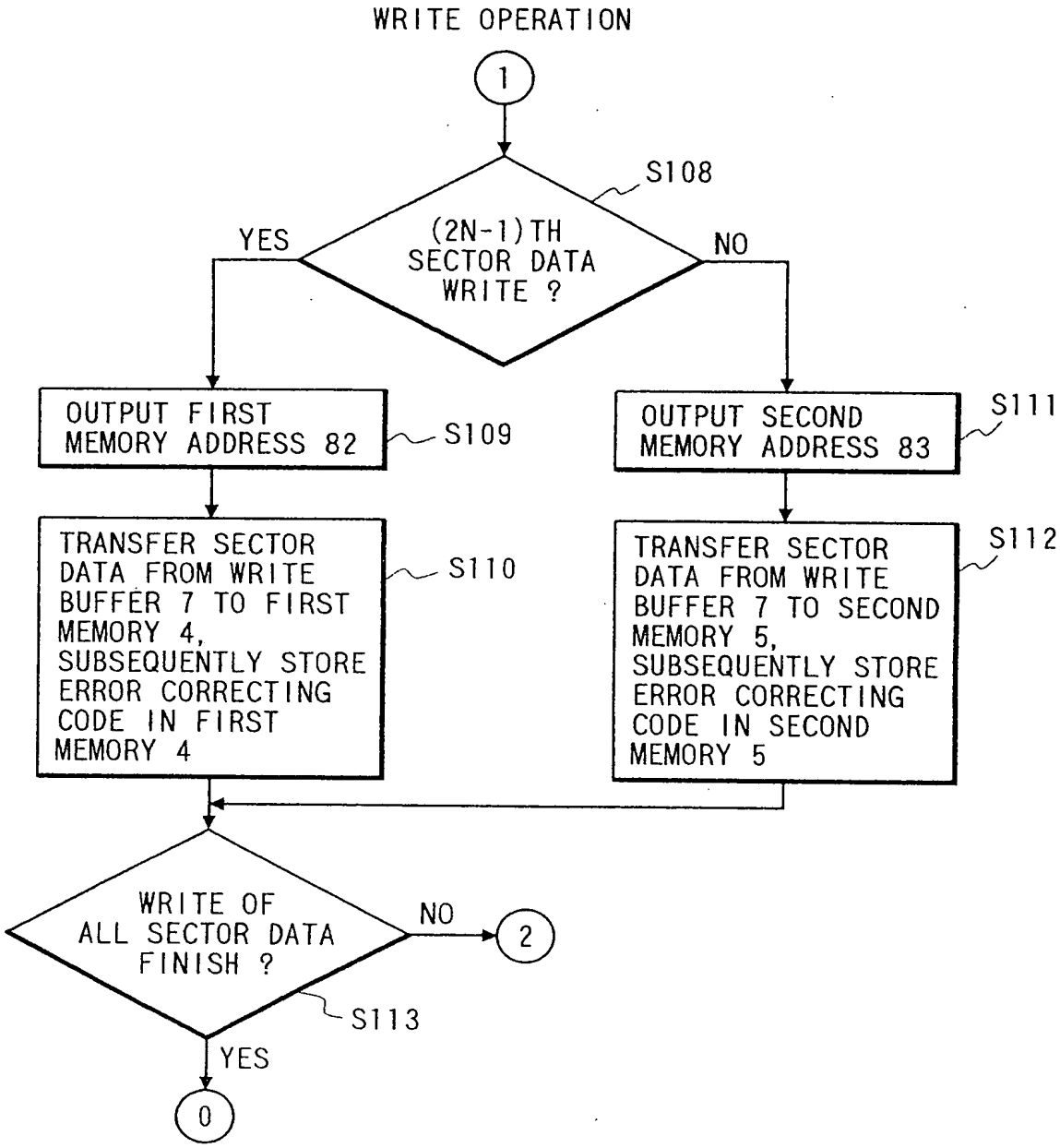
WRITE OPERATION
1
S108
(2N-1)TH SECTOR DATA WRITE ?
YES
NO
OUTPUT FIRST MEMORY ADDRESS 82
S109
OUTPUT SECOND MEMORY ADDRESS 83
S111
TRANSFER SECTOR DATA FROM WRITE BUFFER 7 TO FIRST MEMORY 4, SUBSEQUENTLY STORE ERROR CORRECTING CODE IN FIRST MEMORY 4
S110
TRANSFER SECTOR DATA FROM WRITE BUFFER 7 TO SECOND MEMORY 5, SUBSEQUENTLY STORE ERROR CORRECTING CODE IN SECOND MEMORY 5
S112
WRITE OF ALL SECTOR DATA FINISH ?
NO
2
S113
YES
0

FIG. 9

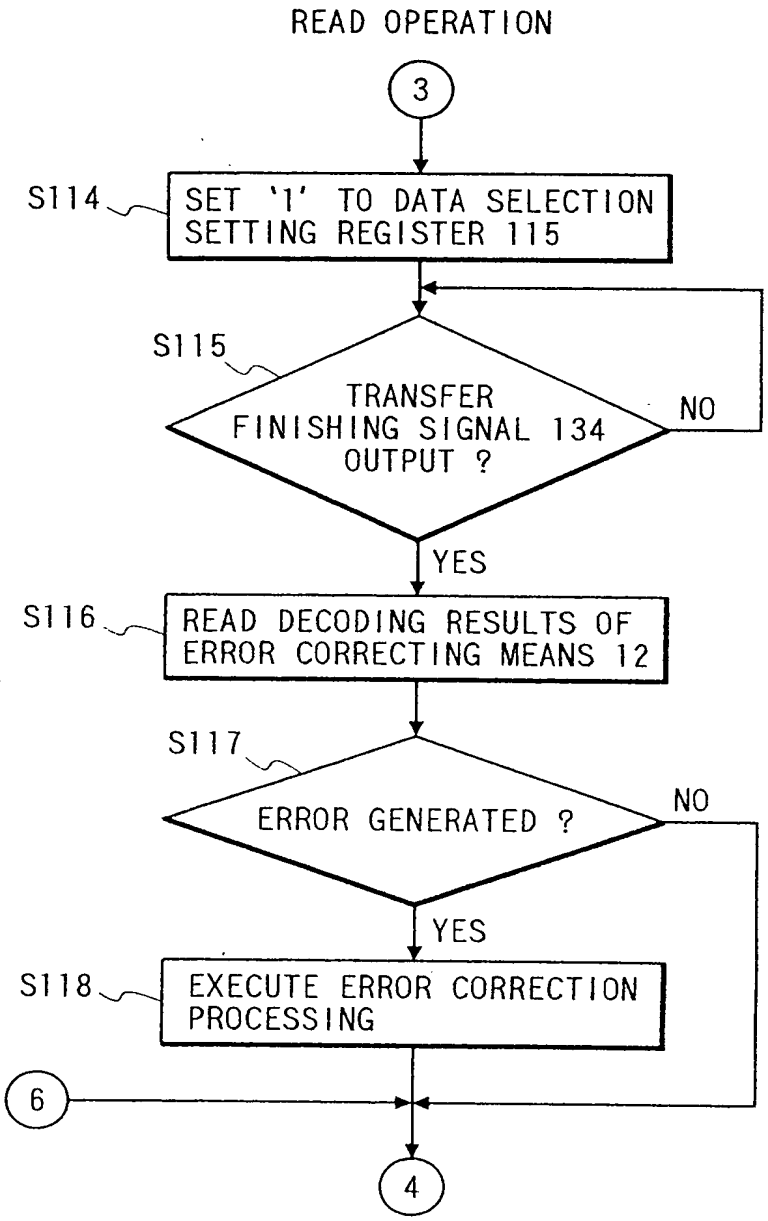
READ OPERATION
3
S114
SET '1' TO DATA SELECTION SETTING REGISTER 115
S115
TRANSFER FINISHING SIGNAL 134 OUTPUT ?
NO
YES
S116
READ DECODING RESULTS OF ERROR CORRECTING MEANS 12
S117
ERROR GENERATED ?
NO
YES
S118
EXECUTE ERROR CORRECTION PROCESSING
6
4

FIG. 10

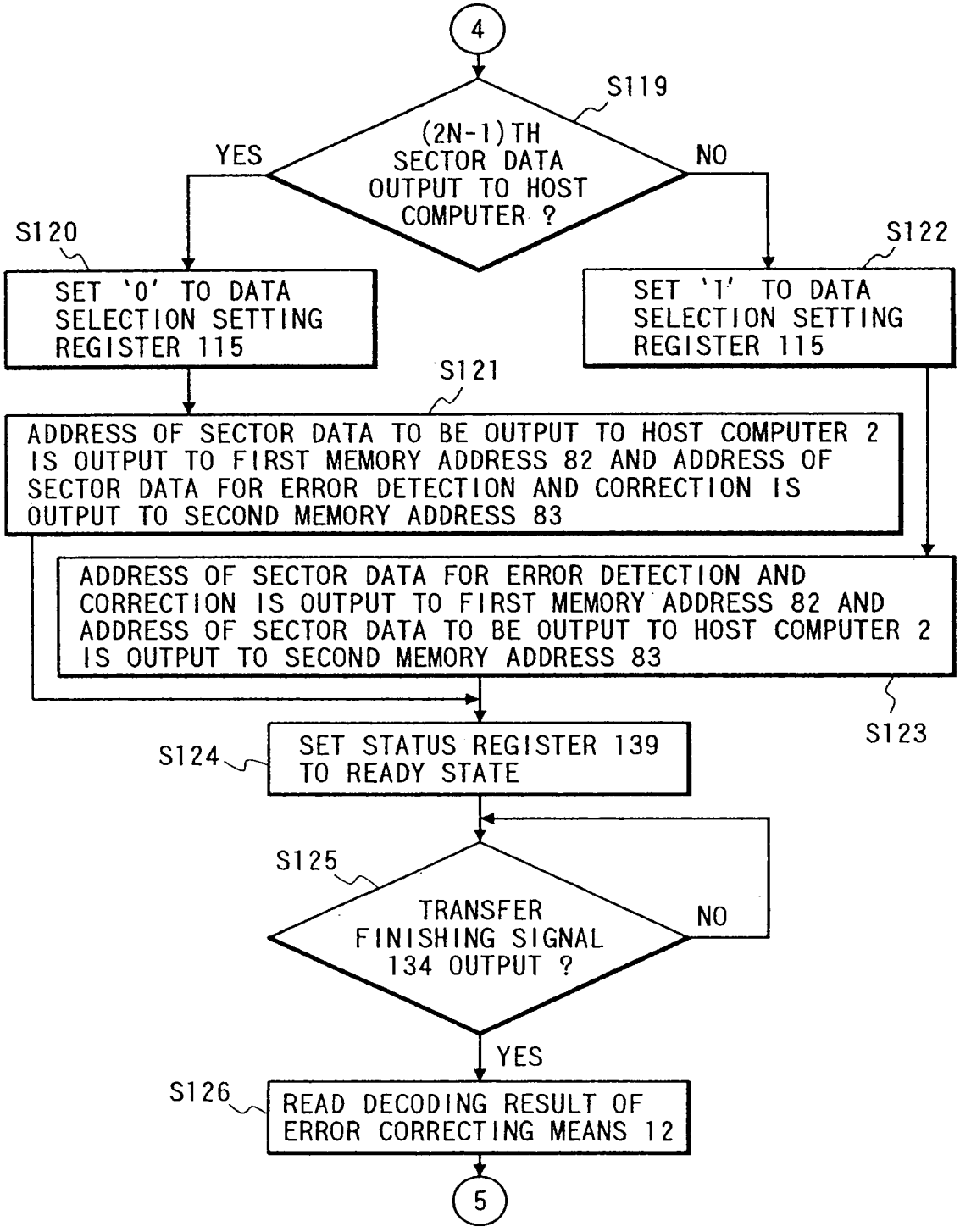
4
S119
(2N-1)TH SECTOR DATA OUTPUT TO HOST COMPUTER ?
YES
NO
S120
SET '0' TO DATA SELECTION SETTING REGISTER 115
S122
SET '1' TO DATA SELECTION SETTING REGISTER 115
S121
ADDRESS OF SECTOR DATA TO BE OUTPUT TO HOST COMPUTER 2 IS OUTPUT TO FIRST MEMORY ADDRESS 82 AND ADDRESS OF SECTOR DATA FOR ERROR DETECTION AND CORRECTION IS OUTPUT TO SECOND MEMORY ADDRESS 83
ADDRESS OF SECTOR DATA FOR ERROR DETECTION AND CORRECTION IS OUTPUT TO FIRST MEMORY ADDRESS 82 AND ADDRESS OF SECTOR DATA TO BE OUTPUT TO HOST COMPUTER 2 IS OUTPUT TO SECOND MEMORY ADDRESS 83
S123
S124
SET STATUS REGISTER 139 TO READY STATE
S125
TRANSFER FINISHING SIGNAL 134 OUTPUT ?
NO
YES
S126
READ DECODING RESULT OF ERROR CORRECTING MEANS 12
5

FIG. 11

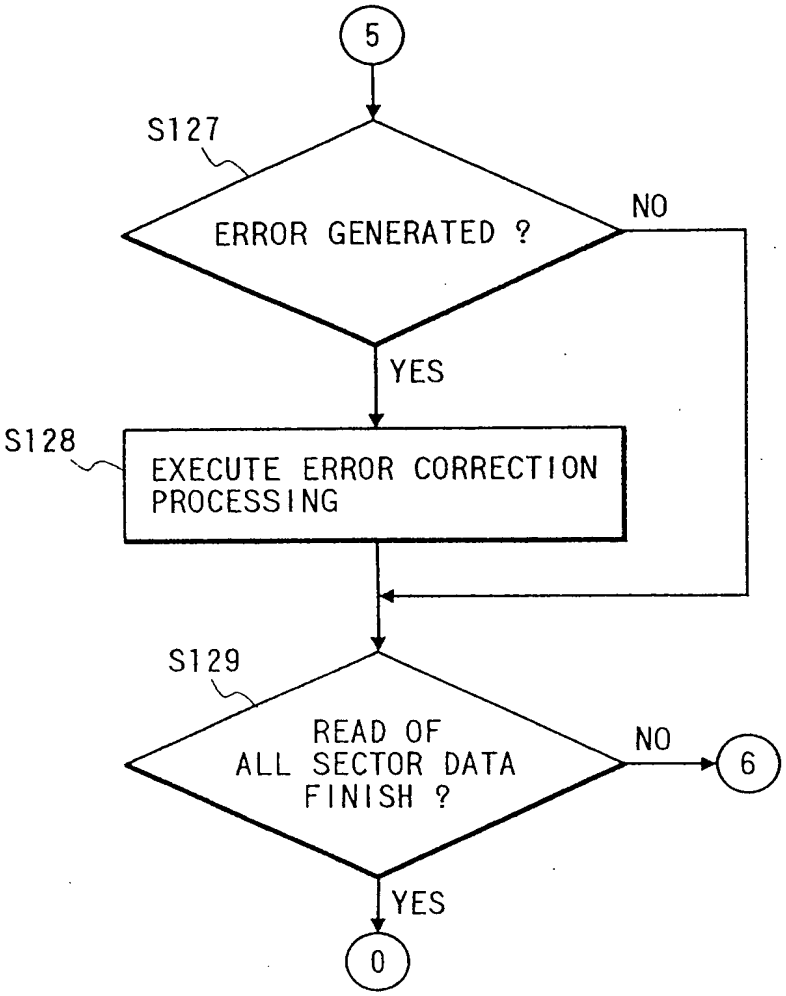
5
S127
ERROR GENERATED ?
NO
YES
S128
EXECUTE ERROR CORRECTION PROCESSING
S129
READ OF ALL SECTOR DATA FINISH ?
NO
6
YES
0

FIG. 12

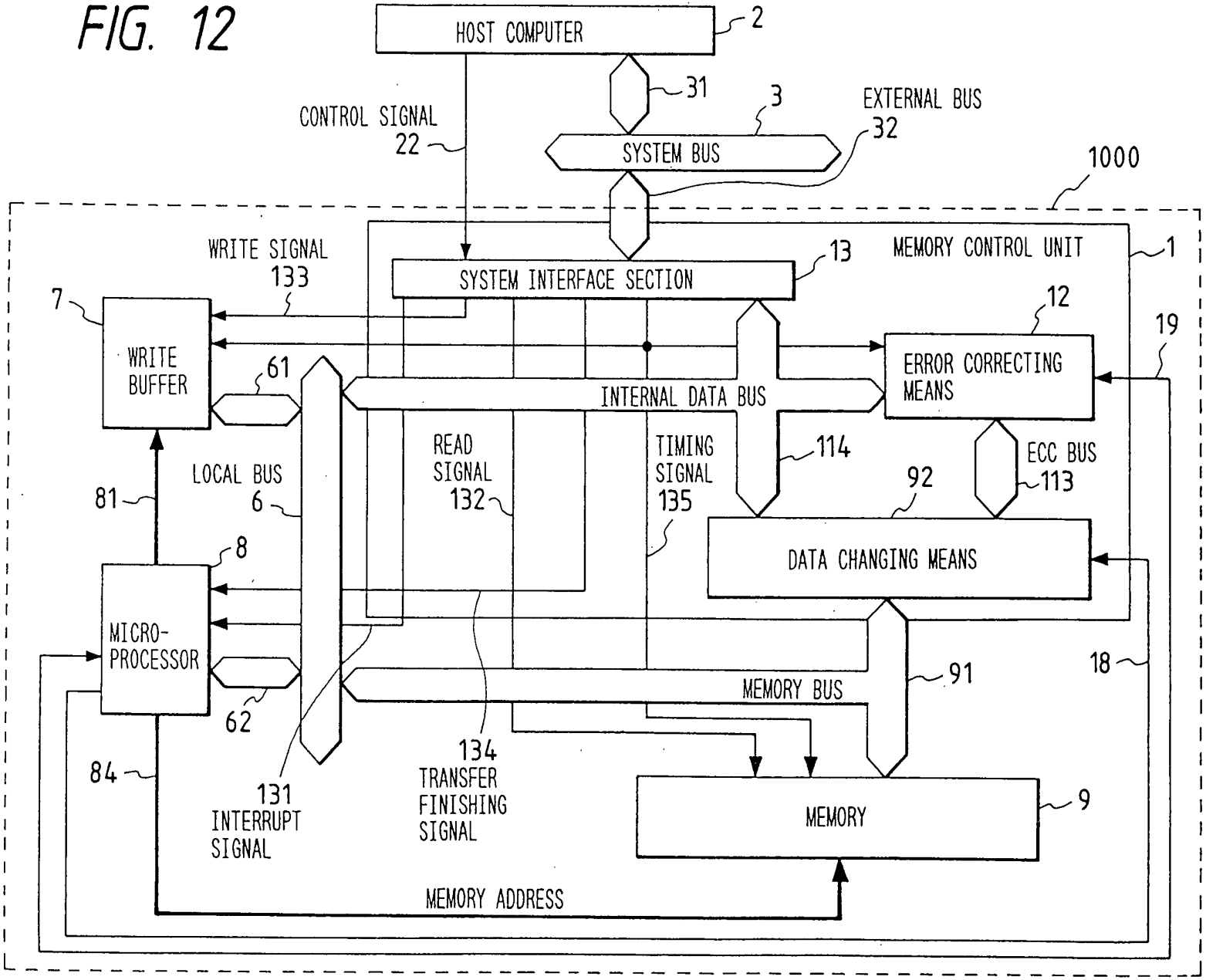
HOST COMPUTER
2
31
3
EXTERNAL BUS
32
CONTROL SIGNAL
22
SYSTEM BUS
1000
MEMORY CONTROL UNIT
1
WRITE SIGNAL
133
SYSTEM INTERFACE SECTION
13
7
12
19
WRITE BUFFER
61
ERROR CORRECTING MEANS
INTERNAL DATA BUS
READ SIGNAL
132
TIMING SIGNAL
135
114
ECC BUS
113
LOCAL BUS
6
81
92
DATA CHANGING MEANS
8
MICRO-PROCESSOR
62
91
18
MEMORY BUS
84
131
INTERRUPT SIGNAL
134
TRANSFER FINISHING SIGNAL
MEMORY
9
MEMORY ADDRESS

FIG. 13

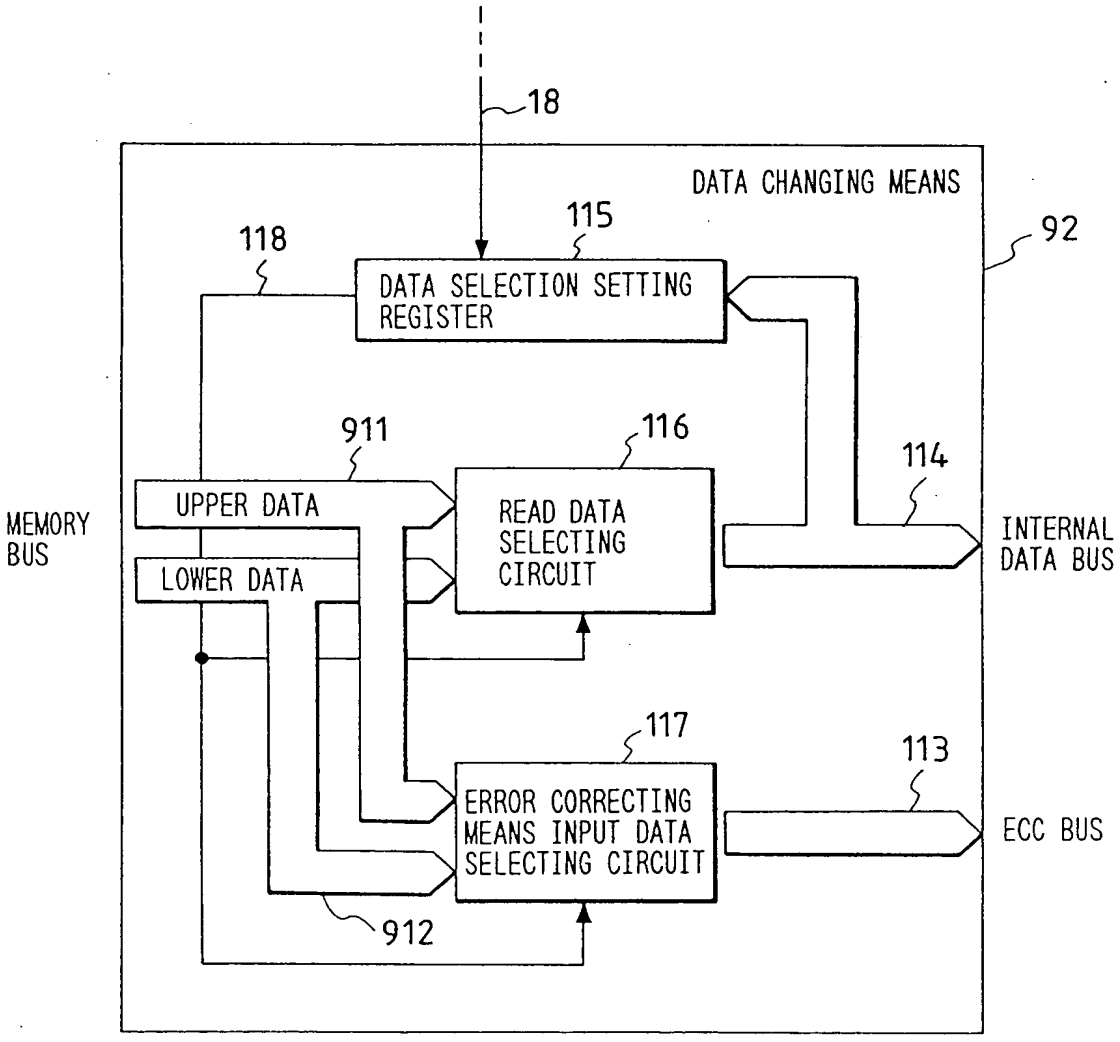
18
DATA CHANGING MEANS
92
115
118
DATA SELECTION SETTING REGISTER
911
116
114
MEMORY BUS
UPPER DATA
LOWER DATA
READ DATA SELECTING CIRCUIT
INTERNAL DATA BUS
117
113
ERROR CORRECTING MEANS INPUT DATA SELECTING CIRCUIT
ECC BUS
912

FIG. 14

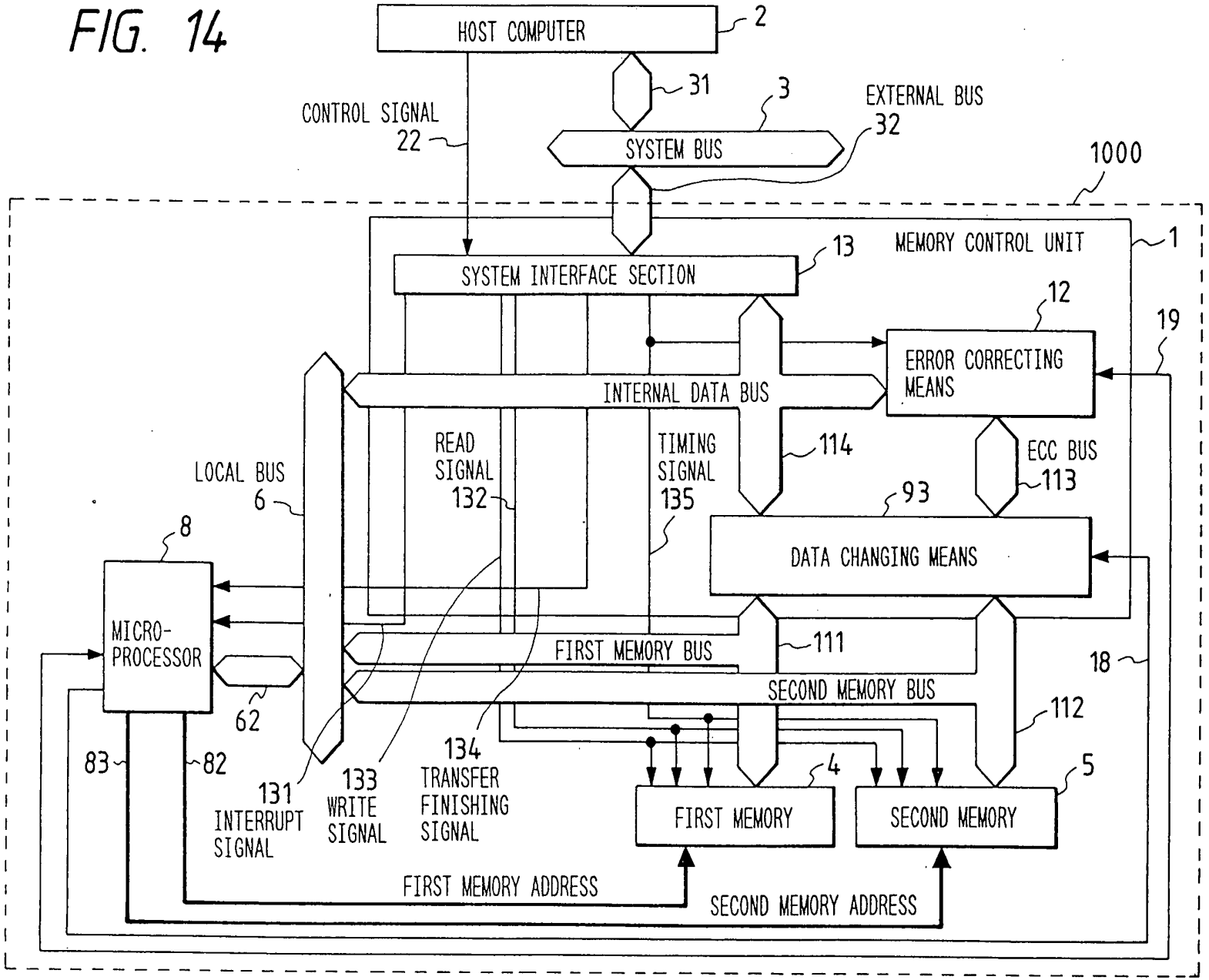
HOST COMPUTER
2
31
3
EXTERNAL BUS
32
CONTROL SIGNAL
22
SYSTEM BUS
1000
MEMORY CONTROL UNIT
1
13
SYSTEM INTERFACE SECTION
12
19
ERROR CORRECTING MEANS
INTERNAL DATA BUS
READ SIGNAL
132
TIMING SIGNAL
135
114
ECC BUS
113
LOCAL BUS
6
93
8
DATA CHANGING MEANS
MICRO-PROCESSOR
FIRST MEMORY BUS
111
18
SECOND MEMORY BUS
112
62
83
82
131
INTERRUPT SIGNAL
133
WRITE SIGNAL
134
TRANSFER FINISHING SIGNAL
4
5
FIRST MEMORY
SECOND MEMORY
FIRST MEMORY ADDRESS
SECOND MEMORY ADDRESS

FIG. 15

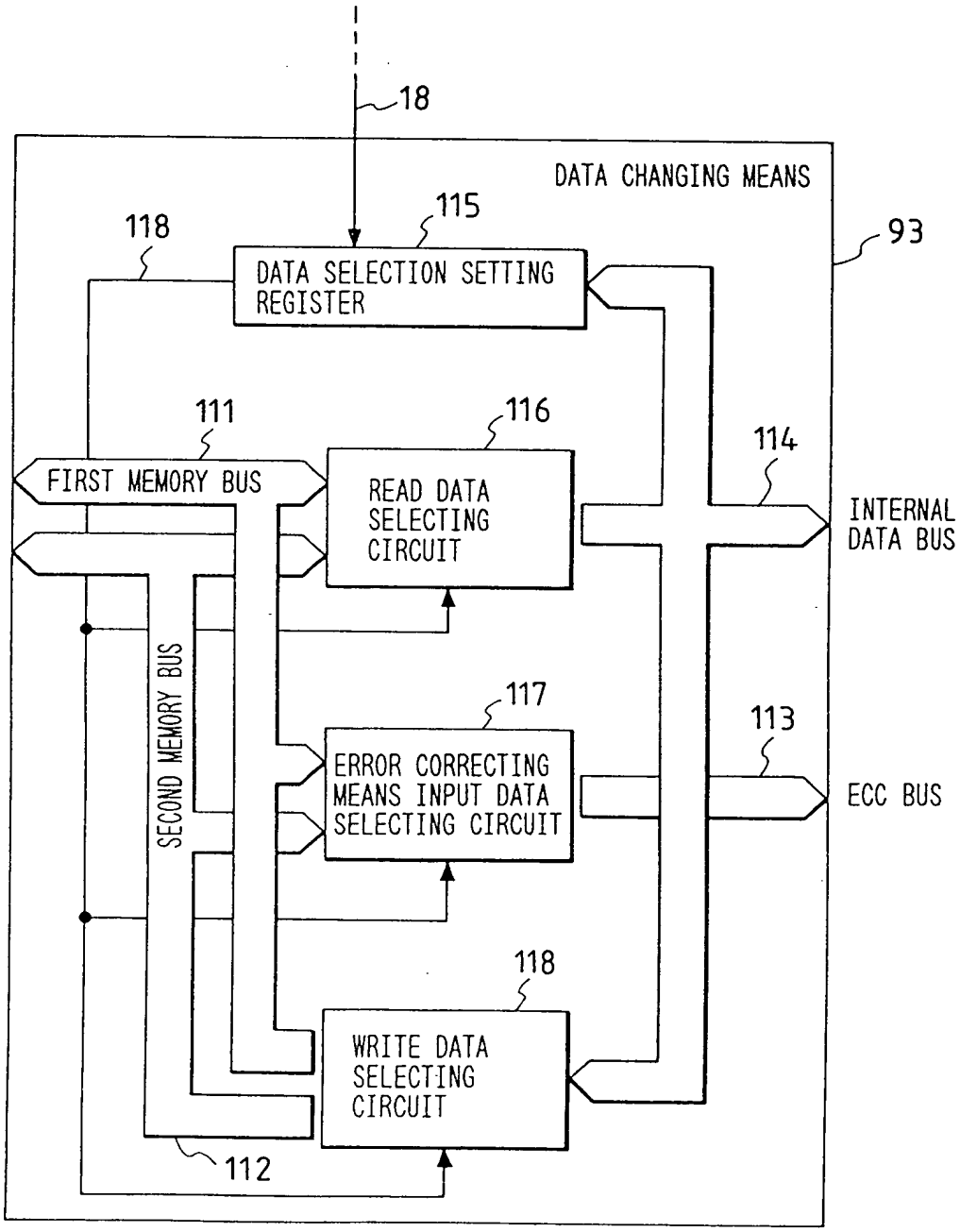
18
DATA CHANGING MEANS
93
118
115
DATA SELECTION SETTING REGISTER
111
116
114
FIRST MEMORY BUS
READ DATA SELECTING CIRCUIT
INTERNAL DATA BUS
SECOND MEMORY BUS
117
113
ERROR CORRECTING MEANS INPUT DATA SELECTING CIRCUIT
ECC BUS
118
WRITE DATA SELECTING CIRCUIT
112

FIG. 16

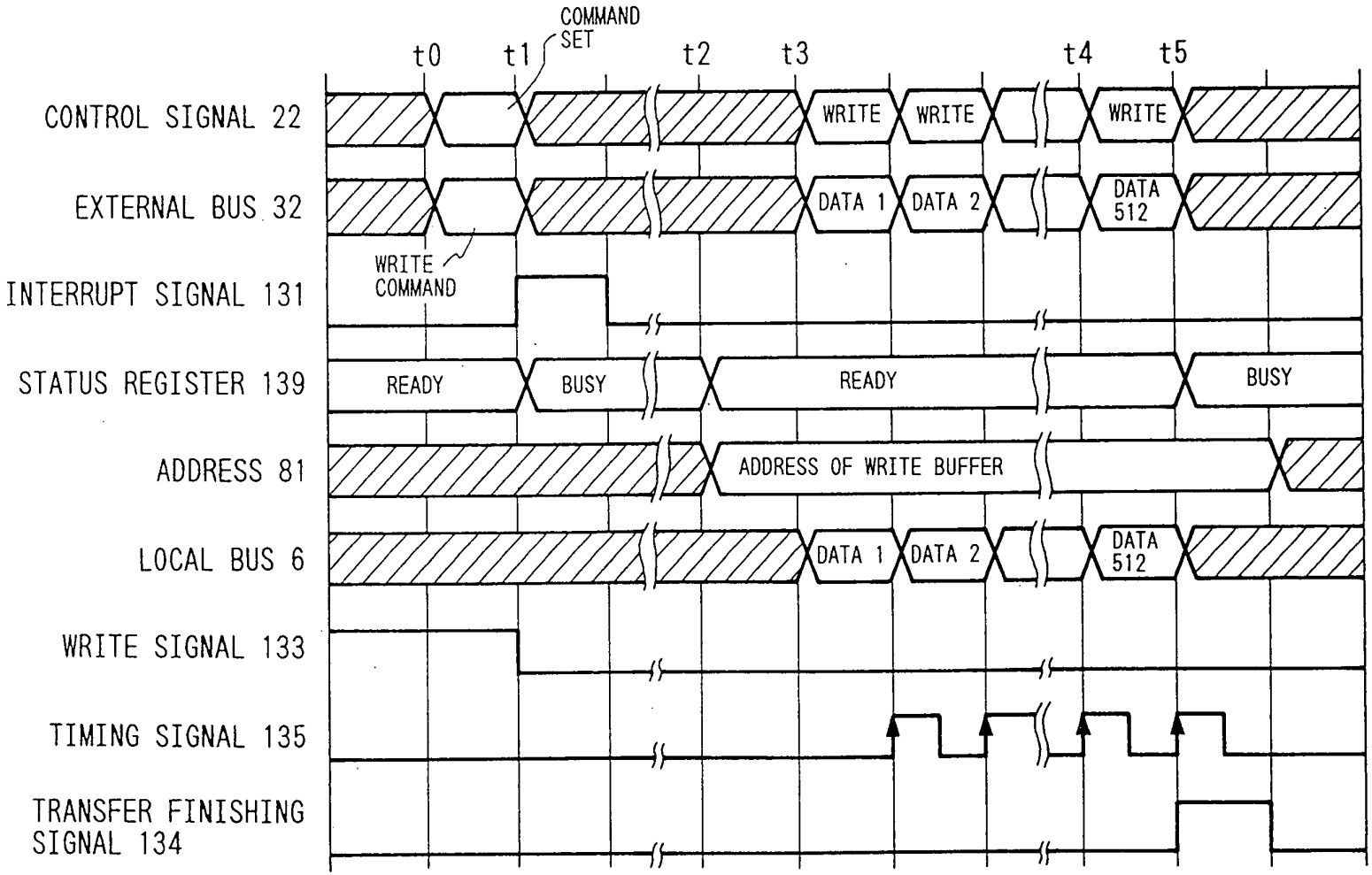
COMMAND SET
t0
t1
t2
t3
t4
t5
CONTROL SIGNAL 22
EXTERNAL BUS 32
INTERRUPT SIGNAL 131
STATUS REGISTER 139
ADDRESS 81
LOCAL BUS 6
WRITE SIGNAL 133
TIMING SIGNAL 135
TRANSFER FINISHING SIGNAL 134
WRITE
WRITE
WRITE
DATA 1
DATA 2
DATA 512
WRITE COMMAND
READY
BUSY
READY
BUSY
ADDRESS OF WRITE BUFFER
DATA 1
DATA 2
DATA 512

FIG. 17

FIRST MEMORY 4

ADDRESS							
100	DATA 1-1	DATA 1-2	-------	DATA 1-512	CODE 1-1	CODE 1-2	CODE 1-3	1ST SECTOR DATA
102	DATA 3-1	DATA 3-2	-------	DATA 3-512	CODE 3-1	CODE 3-2	CODE 3-3	3RD SECTOR DATA

CODE

SECOND MEMORY 5

ADDRESS							
101	DATA 2-1	DATA 2-2	-------	DATA 2-512	CODE 2-1	CODE 2-2	CODE 2-3	2ND SECTOR DATA
103	DATA 4-1	DATA 4-2	-------	DATA 4-512	CODE 4-1	CODE 4-2	CODE 4-3	4TH SECTOR DATA

FIG. 18

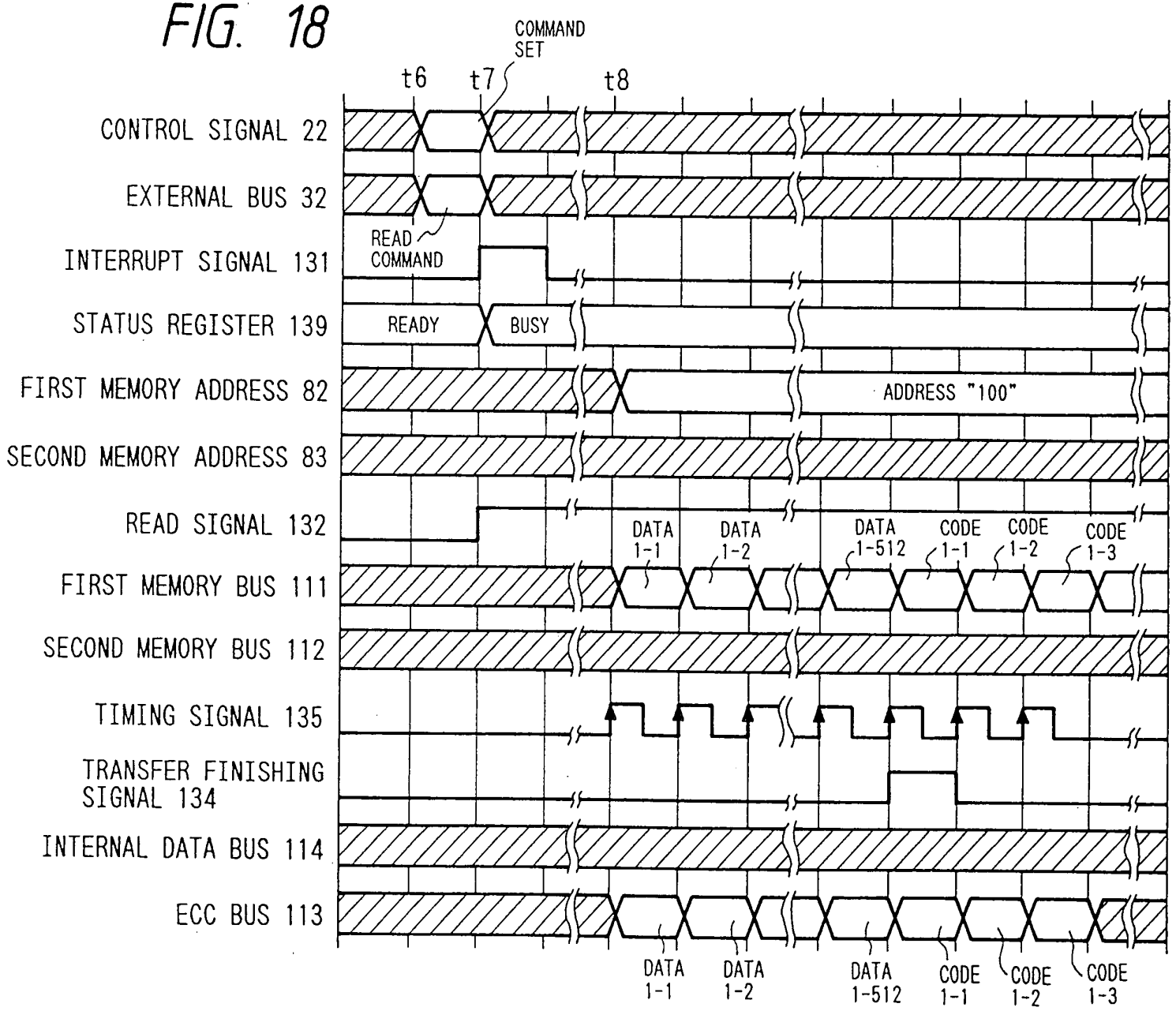
COMMAND SET
t6
t7
t8
CONTROL SIGNAL 22
EXTERNAL BUS 32
READ COMMAND
INTERRUPT SIGNAL 131
STATUS REGISTER 139
READY
BUSY
FIRST MEMORY ADDRESS 82
ADDRESS "100"
SECOND MEMORY ADDRESS 83
READ SIGNAL 132
DATA 1-1
DATA 1-2
DATA 1-512
CODE 1-1
CODE 1-2
CODE 1-3
FIRST MEMORY BUS 111
SECOND MEMORY BUS 112
TIMING SIGNAL 135
TRANSFER FINISHING SIGNAL 134
INTERNAL DATA BUS 114
ECC BUS 113
DATA 1-1
DATA 1-2
DATA 1-512
CODE 1-1
CODE 1-2
CODE 1-3

FIG. 19

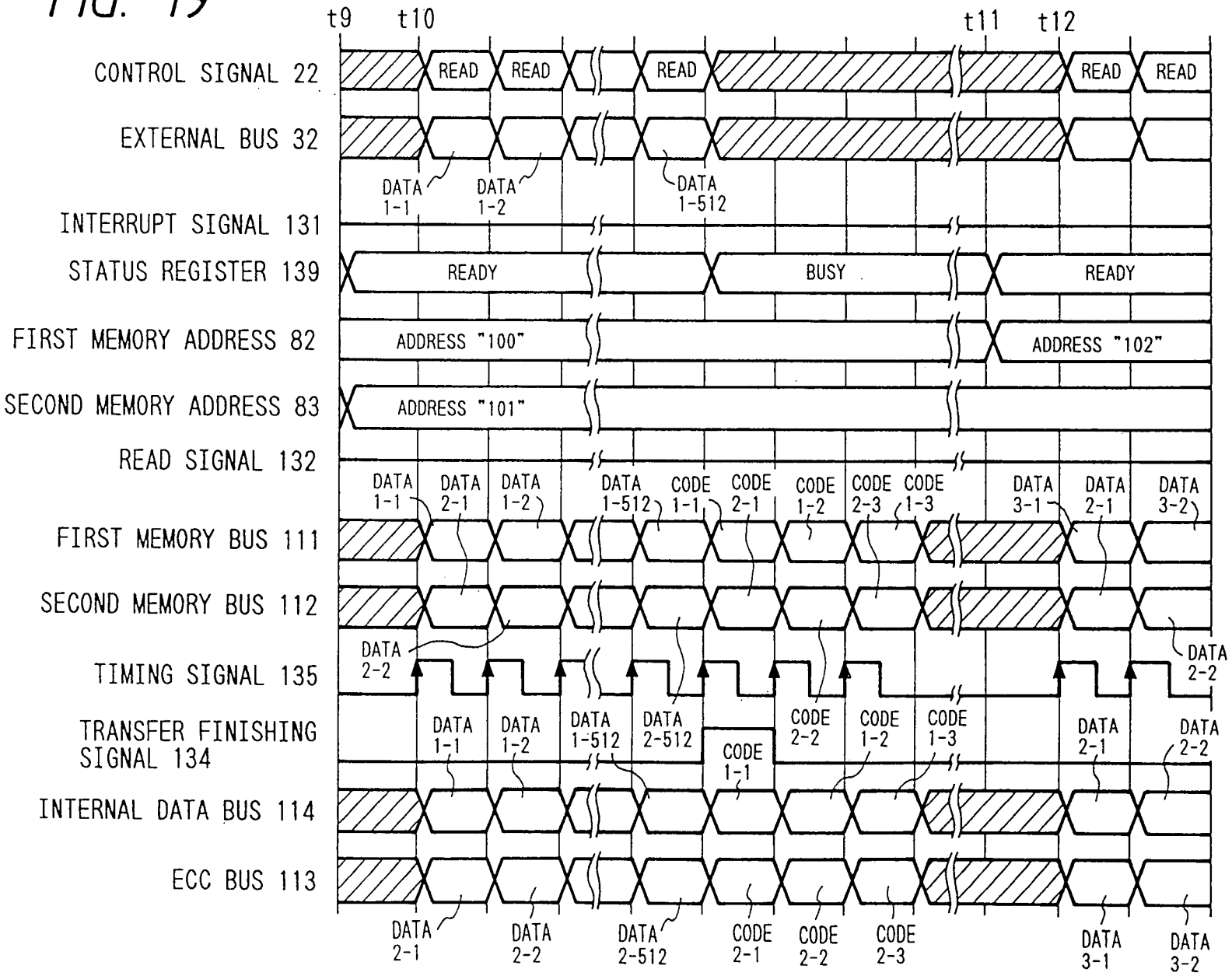
t9
t10
t11
t12
CONTROL SIGNAL 22
READ
READ
READ
READ
READ
EXTERNAL BUS 32
DATA 1-1
DATA 1-2
DATA 1-512
INTERRUPT SIGNAL 131
STATUS REGISTER 139
READY
BUSY
READY
FIRST MEMORY ADDRESS 82
ADDRESS "100"
ADDRESS "102"
SECOND MEMORY ADDRESS 83
ADDRESS "101"
READ SIGNAL 132
FIRST MEMORY BUS 111
SECOND MEMORY BUS 112
TIMING SIGNAL 135
TRANSFER FINISHING SIGNAL 134
INTERNAL DATA BUS 114
ECC BUS 113
DATA 1-1
DATA 2-1
DATA 1-2
DATA 1-512
CODE 1-1
CODE 2-1
CODE 1-2
CODE 2-3
CODE 1-3
DATA 3-1
DATA 2-1
DATA 3-2
DATA 2-2
DATA 1-1
DATA 1-2
DATA 1-512
DATA 2-512
CODE 1-1
CODE 2-2
CODE 1-2
CODE 1-3
DATA 2-1
DATA 2-2
DATA 2-1
DATA 2-2
DATA 2-512
CODE 2-1
CODE 2-2
CODE 2-3
DATA 3-1
DATA 3-2

FIG. 20